

TIMOTHY M. CREECH

CONTACT INFORMATION

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EDUCATION

Ph.D., Electrical Engineering University of Maryland, College Park December 2015. GPA: 4.0.
M.S., Electrical Engineering University of Maryland, College Park May 2015. GPA: 4.0.
B.S., Computer Engineering University of Maryland, College Park May 2009. GPA: 3.67.

TECHNICAL SKILLS

- Extensive experience in parallel runtimes and compilers, particularly using the LLVM compiler infrastructure.
- Experience with system-level programming within and for UNIX-like operating systems, particularly toward concurrency and parallelism.
- Strong familiarity with UNIX-like operating systems, particularly Linux, FreeBSD, and Illumos-based systems.
- Familiarity with hardware- and OS-level virtualization technologies, including KVM, Docker, jails, and zones.

RESEARCH EXPERIENCE

NASA Space Technology Research Fellow September 2011 to August 2015
Visiting Technologist, PhD Student

- Designed, implemented, and evaluated “SCAF,” a new technique for multiprogramming malleable parallel processes on shared-memory computers. Published results in MICRO46; launched website with open-source implementation at <http://scaf.ece.umd.edu>. At NASA Goddard, applied SCAF techniques to the Tiler TileGX as a proxy for future space-bound multiprocessor platforms, and improved Linux’s cache management heuristics for TileGX. At NASA Ames, ported SCAF to the Intel Xeon Phi 5110p, identifying multiprogramming challenges specific to the Phi.
- Collaborated with another graduate student at UMD to design, implement and evaluate “AESOP”, an auto-parallelizing compiler for shared-memory computers based on LLVM. Produced a website with open-source implementation, interactive demo, and whitepaper at <http://aesop.ece.umd.edu>. At NASA Goddard, ported AESOP to the Tiler TileGX.
- At NASA Goddard, supported development of a prototype intelligent payload module for air- and space-bound instruments based on Tiler multiprocessors and Xilinx processor-centric FPGA platforms. Guided engineers with integrating new data processing applications into the TilePro/Linux platform, and helped to design the payload module’s internal networking, storage, and processing architecture.

NASA, Goddard Space Flight Center June 2011 to August 2011
Graduate Intern

- Researched the performance of the 64-core Tile64 processor in the context of single-process, multithreaded parallelism. Identified the most significant obstacles to scalability for multithreaded programs, runtime systems, and compilers. Modified the Tile64 Linux kernel to accept dynamic hints from userspace about where best to cache memory allocations.
- Began improving AESOP’s support for Tile64, working toward automated parallelization of a large suite of space-bound software. Created LLVM analysis and code generation passes to provide cache homing hints to the Tile64 Linux kernel.

University of Maryland, Electrical and Computer Engineering Dept. January 2011 to May 2011
Research Assistant

- Research advisor: Dr. Rajeev Barua
- Participated in early DARPA-funded development of AESOP, which strove to intelligently integrate integrate serial, autoparallelizing, affine, and non-affine compiler techniques within a single compiler.

PROFESSIONAL EXPERIENCE

SecondWrite, LLC January 2016 to present
Principal Software Engineer

- Building next-generation tools for application performance monitoring.

ARINC - GLOBALink Engineering
Engineer

June 2009 to August 2010

- Advanced development on a real-time traffic monitor for a global, mission-critical ARINC network.
- Developed a Linux-based radio ground station platform to replace proprietary single-board-computer systems.

University of Maryland Institute for Advanced Computer Studies
Student Administrator/Technician

October 2007 to May 2009

- Performed administration of a large-scale, heterogeneous system of computers as part of a team; included network, systems, and datacenter maintenance.
- Maintained a wide variety of machines running Linux, Sun Solaris, and Microsoft Windows.
- Provided help-desk support to UMIACS students, faculty, and staff.

ARINC - GLOBALink Engineering
Intern

June 2008 to August 2008

- Advanced the migration of a real-time monitoring system from Solaris on SPARC to GNU/Linux on x86.
- Performed rigorous testing on the above monitoring system in order to work towards high availability.
- Maintained a number of internal tools written in Coldfusion.

TEACHING EXPERIENCE

University of Maryland, Electrical and Computer Engineering Dept.
Teaching Assistant

September 2010 to December 2010

- Assisted Prof. Yavuz Oruç with ENEE350, "Computer Organization."
- Designed and conducted discussion sections, held office hours, and graded all assignments and examinations.

HONORS, AWARDS, AND OTHER EXPERIENCE

- NASA Space Technology Research Fellow, September 2011 through August 2015.
- Volunteer <http://mirror.umd.edu> maintainer since May 2013.
- Finalist in the Booz Allen Hamilton Tech Challenge for UMD, 2009.
- Included in the Dean's List of Students for 6 semesters (Fall 2006 through Spring 2009).
- Invited to the University of Maryland's Electrical and Computer Engineering Honors Program in Fall 2007.
- Performing Member of the University of Maryland's flagship Symphony Orchestra from September 2005 to May 2007.
- Awarded the Director's Scholarship for Music Performance, September 2005 to May 2007.

PUBLICATIONS

- [1] T. Creech, A. Kotha, and R. Barua, "Efficient multiprogramming for multicores with SCAF," in *Proceedings of the 46th Annual IEEE/ACM International Symposium on Microarchitecture ("MICRO46;"* 16% acceptance rate). ACM, 2013, pp. 334–345.
- [2] A. Kotha, T. Creech, and R. Barua, "AESOP: The autoparallelizing compiler for shared memory computers," Available at <http://aesop.ece.umd.edu/>, University of Maryland, College Park, Tech. Rep., 2013.
- [3] A. Kotha, K. Anand, T. Creech, K. ElWazeer, M. Smithson, and R. Barua, "Affine parallelization of loops with runtime dependent bounds from binaries," in *Programming Languages and Systems ("ESOP 2014;"* 24% acceptance rate). Springer Berlin Heidelberg, 2014, pp. 554–574.
- [4] A. Kotha, K. Anand, T. Creech, K. ElWazeer, M. Smithson, G. Yellareddy, and R. Barua, "Affine parallelization using dependence and cache analysis in a binary rewriter," *IEEE Transactions on Parallel and Distributed Systems*, 2014.